MALLA REDDY ENGINEERING COLLEGE

(Autonomous)

Maisammaguda, Dhulapally,Secunderabad – 500100

II B.Tech I Semester, CSE(AIML)

Mid Term Examinations-I

Subject Code & Name: - **C0509 & Computer Organization and Architecture**

Marks: **25M** Time: **90 Mins**

Answer ALL the Questions Date:

S. No.	Questions	Marks	BT Level	CO
	Module-1			
1	Sketch a neat diagram and explain in detail the functional units of a computer.	5	2	1
2	Describe Bus and Memory Transfers	5	2	1
3	Explain the one stage of arithmetic logic shift unit with a neat sketch.	5	3	1
4	Classify different logic micro operations with the functional table.	5	2	1
5	Demonstrate different shift micro operations in detail.	5	2	1
6	Write about Computer Design and Computer Architecture	5	3	1
7	Explain the different memory reference instructions	5	2	1
8	Explain Input – Output and Interrupt	5	2	1

S.No.	Questions	Marks	BT Level	CO
	Module-2			
1	Explain briefly about control memory	5	3	2
2	Describe Micro Program with an example	5	2	2
3	Explain about address sequencing capabilities in control memory.	5	2	2
4	Distinguish between data transfer and data manipulation instructions.	5	2	2
5	Use different instruction format and evaluate the expression Y=(A-B)/(C+D*E)	5	2	2
6	Explain about Addressing Modes with an Numerical Example?	5	2	2
7	Illustrate about General Register Organization	5	2	2
8	Define an instruction? Explain the instruction cycle.	5	2	2

S.No.	Questions	Marks	BT Level	CO
	Module-3			
1	Explain the fixed point representation and floating point representation?	5	2	3
2	Design the flow chart for Booths Multiplication algorithm with an example?	5	2	3
3	Write about Computer Arithmetic Addition with neat flow chart.	5	2	3
4	Illustrate Decimal Arithmetic Unit and Operations	5	2	3

Course Instructor Name: Dr. U. Mohan Srinivas

Signature: **HOD Signature**

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OBJECTIVE QUESTION BANK

Answer ALL the Questions

S.NO.	Questions	Ans
	Module-1	
1	Which sequential circuits generate the feedback path due to the cross-coupled connection from output of one gate to the input of another gate? a)Synchronous b) Asynchronous c) Both d) None of the above	B
2	What is/are the crucial function/s of memory elements used in the sequential circuits? a) Storage of binary information b)Specify the state of sequential c) Both a & b d) None of the above	C
3	How are the sequential circuits specified in terms of time sequence? a) By Inputs b) By Outputs c) By Internal states d)All of the above	D
4	The behavior of synchronous sequential circuit can be predicted by defining the signals at a) discrete instants of time b) continuous instants of time c) sampling instants of time d) at any instant of time	A
5	Which memory elements are utilized in an asynchronous & clocked sequential circuits respectively? a) Time- delay devices & registers b) Time- delay devices & flip-flops c) Time- delay devices & counters d) Time-delay devices & latches	B
6	Why do the D-flip-flops receives its designation or nomenclature as 'Data Flipflops' ? a) Due to its capability to receive data from flip-flop b) Due to its capability to store data in flip-flop c) Due to its capability to transfer the data into flip-flop d) None of this	C
7	The characteristic equation of D-flip-flop implies that a) the next state is dependent on previous state b) the next state is dependent on present state c) the next state is independent of previous state d) the next state is independent of present stated	D
8	Which circuit is generated from D-flip-flop due to addition of an inverter by causing reduction in the number of inputs? a) Gated JK- latch b) Gated SR- latch c) Gated T- latch d) Gated D- latch	D
9	What is the bit storage binary information capacity of any flip-flop? a) 1 bit b) 2 bits c) 16 bits d) infinite bits	A
10	What is/are the directional mode/s of shifting the binary information in a shift register? a) Up-Down b) Left – Right c) Front – Back d) All of the above	B
11	Which time interval specify the shifting of overall contents of the shift registers? a) Bit time b) Shift time c) Word time d) Code time	C
12	A counter is fundamentally a _____ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it. a) Register b) memory unit c) Flip-flop d) arithmetic logic unit	C

13	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? a) 0 to 2n b) 0 to 2n-1 c) 0 to 2n+1 d) 0 to 2n+1 / 2	B
14	Which property of unit distance counters has the potential to overcome the consequences of multi-bit change flashing that arises in almost all conventional binary and decimal counters? a) one bit change per unit change b) two bits change per unit change c) three bits change per unit change d) four bits change per unit change	A
15	What contributes to the triggering of clock pulse inputs for all the flip-flops excluding the first flip-flop in a ripple counter? a) Incoming Pulses b) Output Transition c) Double Clock Pulses d) All of the above	B
16	What is the required relationship between number of flip-flops and the timing signals in Johnson Counter? a) No. of flip-flops = 1/2 x No. of timing signals b) No. of flip-flops = 2/3 x No. of timings signals c) No. of flip-flops = 3/4 x No. of timing signals d) No. of flip-flops = 4 x No. of timing signals	A
17	Which clock pulses are generated by the microprocessor so as to handle the timing and control operations related to internal functioning level? a) single phase clock pulses b) multi-phase clock pulses c) anti-phase clock pulses d) none of the above	B
18	The bus-request control input of micro-processor indicates the temporary suspension of current operation by driving all buses into_____. a) high impedance state b) low impedance state c) both a & b d) none of the above	A
19	Which feature conducts the memory transfer by controlling the address and data buses on the basis of request originated by the device when buses get disabled by the microprocessor? a) Indirect Memory Access b) Direct Memory Access c) Read Memory Access d) Write Memory Access	B
20	By default counters are incremented by a) 1 b) 2 c) 3 d) 4	A
21	Simplest registers only consists of a) Counter b) EPROM c) Latch d) flip-flop	D
22	Three decade counter would have a) 2 BCD counters b) 3 BCD counters c) 4 BCD counters d) 5 BCD counters	B
23	A decimal counter has a) 5 states b) 10 states c) 15 states d) 20 states	B
24	Memory that is called a read write memory is a) ROM b) EPROM c) RAM d) Registers	C
25	2 left shifts are referred to as multiplication with a) 2 b) 4 c) 8 d) 16	B
26	Ripple counters are also called a) SSI counters b) asynchronous counters c) synchronous counters d) VLSI counters	B
27	Transformation to information into registers is called a) Loading b) gated latch c) Latch d) Storing	A
28	Binary counter that count incrementally and decrementally is called a) up-down counter b) LSI counters c) down counter d) up counter	A
29	Shift registers having four bits will enable shift control signal for a) 2 clock pulses b) 3 clock pulses c) 4 clock pulses d) 5 clock pulses	C
30	A group of binary cells is called a) Counter b) Register c) Latch d) Flip-flop	B
31	Synchronous counter is a type of a) SSI counters b) LSI counters c) MSI counters d) VLSI counters	C

32	BCD counter is also known as a) parallel counter b) decade counter c) synchronous counter d) VLSI counter	B
33	A 8-bit flip-flop will have a) 2binary cells b) 4binary cells c) 6binary cells d) 8binary cells	D
34	Parallel load transfer is done in a) 1 cycle b) 2 cycle c) 3 cycle d) 4 cycle	A
35	To start counting enable input should be a) 0 b) 1 c) Reset d) Clear	B
36	Ripple counter cannot be described by a) Boolean equation b) clock duration c) Graph d) flow chart	A
37	Time between clock pulses are called a) bit duration b) clock duration c) Duration d) bit time	D
38	Parallel loading is done in a) 1 cycle b) 2 cycle c) 3 cycle d) 4 cycle	A
39	Control unit in serial computer generates a(B) a) reset signal b) word-time signal c) word signal d) clear signal	B
40	BCD counter counts from a) 0 to 5 b) 1 to 5 c) 0 to 9 d) 1 to 9	C
41	J=K=0 will make flip-flops a) Changed b) Reversed c) Unchanged d) Stopped	C
42	Special type of registers are a) Latch b) Flip-flop c) Counters d) Memory	C
43	Flip-flops in registers are a) Present b) level triggered c) edge triggered d) not present	C
44	Down counter decrement value by a) 1 b) 2 c) 3 d) 4	A
45	Ripple counter is a type of a) SSI counters b) LSI counters c) MSI counters d) VLSI counters	C
46	Propagation of signal through counters is in a) ripple fashion b) serial fashion c) parallel fashion d) both a and b	A
47	Register shifting left and right both is called a) unidirectional shift register b) bidirectional shift register c) left shift register d) right shift register	B
48	A decimal counter has a) 2 flip-flops b) 3 flip-flops c) 4 flip-flops d) 5 flip-flops	C
49	Control variable of registers is also called a) store control input b) load control input c) store control output d) load control output	B
50	Time to transfer content of shift register is called a) word duration b) clock duration c) Duration d) bit time	A
	Module-2	
51	Fast electronic machine accepts digital input information process and produce resulting output is a) Analog Computer b) Digital Computer c) Workstation d) Super Computer	B
52	List of Instructions is a) Computer Program b) Function c) Procedure d) Sub Routine	A
53	Internal Storage is called a) Computer Memory b) Stack c) Queue d) Data structure	A
54	Computer used in home, office and schools is a) Super Computer b) Mainframe Computer c) Personal Computer d) Client machine	C
55	Computer having High resolution graphics I/O capability a) Desktop Computer b) Digital Computer c) Network Computer d) Workstation	D
56	Systems used for business data processing a) Super computers b) Servers c) Mainframe d) Network PC	C

57	Computers used for large scale numerical calculations is a) Super computers b) Servers c) Mainframe d) Network PC	A
58	Systems handling large volumes of requests to access data is a) Super computers b) Servers c) Mainframe d) Network PC	B
59	Computer consists of _____functional independent main parts a) 1 b) 3 c) 5 d) 7	C
60	_____ unit accepts information from human operators a) Output b) Input c) ALU d) Control Unit	B
61	A computer language that is written in binary codes only is _____ a) Machine language b) C c) C# d) Pascal	A
62	Expand ASCII a) American Standard Code for Information Interchange b) American Social code for Instruction Interchange c) Asian standard for Interrupt Interchange d) Asian Stack for Invoice Interchange	A
63	Two classes of storage a) Serial, parallel b) Primary, secondary c) Input, output d) ION,IOF	B
64	ASCII is a ____ bit code a) 1 b) 3 c) 5 d) 7	D
65	Convert the binary equivalent 10101 to its decimal equivalent. a) 21 b) 12 c) 22 d) 31	A
66	Number of bits in each word is referred to as _____ a) Bytelength b) Bitlength c) Wordlength d) Nibblelength	C
67	The time required to access one word is called the a) Memory Read Time b) Memory WriteTime c) Memory Buffer Time d) Memory Access Time	D
68	Basic arithmetic operations are performed in a) CU b) ALU c) Memory d) Input	B
69	_____ sends the processor results to outside world a) Output Unit b) Input Unit c) Memory Unit d) Control Unit	A
70	_____ determines when a given action has to take place a) Clock b) Interval c) Timing Signal d) Pulse	C
71	A group of lines that serve as connecting path for several devices is a) Cable b) Bus c) Wire d) Line	B
72	All activities inside the machine are directed by _____ a) Output Unit b) Input Unit c) Memory Unit d) Control Unit	D
73	_____ is a collection of programs a) Hardware b) System Software c) Circuitry d) Directory	B
74	Expand SCSI a) Small Computer System Interface b) Semi Classic Software Interface c) Semi Circuitry System Interface d) System Computer System Interface	A
75	Important measure of computer is a) System Software b) System Hardware c) Performance d) Bus	C
76	Processor Circuits are controlled by a timing signal called a a) Clock b) Pulse c) FlipFlop d) Registers	A
77	Clock defines regular time intervals called _____ a) Instruction Cycle b) Interrupt Cycle c) Clock Cycle d) Fetch Cycle	C
78	Overlapping the execution of successive instructions called a) Vector Processing b) Pipelining c) Array Processing d) Central Processing	B
79	3 bits full adder contains _____ a) 3 combinational inputs b) 4 combinational inputs c) 6 combinational inputs d) 8 combinational inputs	D
80	_____ translates high level language to machine language a) Assembler b) Router c) Compiler d) Interpreter	C

81	_____ hold the address which is to be accessed a) MDR b) PC c) IR d) MAR	D
82	Operations executed on data stored registers are a) Micro operations b) Mini operaions c) Large scale operations d) Small scale operations	A
83	_____ micro operations are performed on numeric data stored in registers a) Register transfer b) Arithmetic c) Logic d) Shift	B
84	_____ micro operations perform bit manipulation operations on non numeric data stored in registers a) Register transfer b) Arithmetic c) Logic d) Shift	C
85	Addition , Subtraction, Increment and Decrement are a) Register transfer micro operations b) Arithmetic micro operations c) Logic micro operations d) Shift micro operations	B
86	A number of storage registers connected to a common operational unit a) ALU b) CU c) Input d) Output	A
87	The code where all successive numbers differ from their preceding number by single bit is ____ a) Alphanumeric Code b) BCD c) Excess 3 d) Gray	D
88	_____ operation sets to 1 the bits in register A where the corresponding 1's in register B a) Selective Clear b) Selective Set c) Selective Complement d) Selective Reset	B
89	_____ operation complements bits in register A where there are corresponding 1's in register B a) Selective Clear b) Selective Set c) Selective Complement d) Selective Reset	C
90	_____ operation clears to zero the bits in A only where there are corresponding 1's in register B a) Selective Clear b) Selective Set c) Selective Complement d) Selective Reset	A
91	Mask operation is a _____ micro operation a) NAND b) NOR c) AND d) OR	C
92	Insert operation is a _____ micro operation a) NAND b) NOR c) AND d) OR	D
93	Many to one combinational circuit is a) Encoder b) Decoder c) Multiplexer d) Adder	C
94	Expand PC a) Program Counter b) Process Counter c) Program Circuit d) Parity Counter	A
95	Expand IR a) Interrupt Register b) Instruction Register c) Isolated Rate d) Integrated Route	B
96	Expand MDR a) Massive data rate b) Memory Decode Register c) Memory Dual Register d) Memory Data Register	D
97	A bus system can be constructed with a _____ a) One stage gate b) Two stage gate c) Three stage gate d) Four stage gate	C
98	The output which is not being driven to any defined logic level a) Low Impedence state b) High Impedence state c) 0 State d) 1 State	B
99	A group of bits that tell the computer to perform a specific operation is known as____. a) Instruction code b) Micro-operation c) Accumulator d) Register	A
100	The time interval between adjacent bits is called the_____ a) Word-time b) Bit-time c) Turnaround time d) Slice time	B
	Module-3	
101	In micro-programmed approach, the signals are generated by _____.	A

	a) Machine instructions b) System programs c) Utility tools d) None of the above	
102	A word whose individual bits represent a control signal is _____. a) Command word b) Control wordc) Co –ordination word d) Generation word	B
103	A sequence of control words corresponding to a control sequence is called _____. a) Micro routineb) Micro function c) Micro procedure d) None of the above	A
104	Individual control words of the micro routine are called as _____. a) Micro task b) Micro operation c) Micro instruction d) Micro command	C
105	The special memory used to store the micro routines of a computer is _____. a) Control table b) Control store c) Control mart d) Control shop	B
106	To read the control words sequentially _____ is used. a) PC b) IR c) UPC d) None of the above	C
107	Every time a new instruction is loaded into IR the output of _____ is loaded into UPC. a) Starting address generator b) Loader c) Linker d) Clock	A
108	_____ are the different type/s of generating control signals. a) Micro-programmed b) Hardwired c) Micro-instruction d) Both a and b	D
109	The type of control signal are generated based on a) Contents of the step counter b) Contents of IR c) Contents of condition flags d) All of the above	D
110	What does the hardwired control generator consist of? a) Decoder/encoder b) Condition codes c) Control step counter d) All of the above	D
111	What does the end instruction do? a) It ends the generation of a signal b) It ends the complete generation process c) It starts a new instruction fetch cycle and resets the counter d) It is used to shift the control to the processor	C
112	The disadvantage/s of the hardwired approach is a) It is less flexible b) It cannot be used for complex instructions c) It is costly d) Both a and b	D
113	Processors of all computers must have a) ALU b) Primary storage c) Control unit d) All the above	D
114	What is the control unit's function in the CPU a) To transfer data to primary storage b) To store program instruction c) To perform logic operation d) To decode program instruction	D
115	What is meant by a dedicated computer? a) Which is used by one person only b) Which is assigned to one and only one task c) Which does one kind of software d) Which is meant for application software only	B
116	A micro program written as string of 0's and 1's is a a) Symbolic microinstruction b) Binary microinstruction c) Symbolic micro program d) Binary micro program	D
117	When sending an assembly language instruction over a bus, it is put on which lines of the bus a) Control lines b) Cache lines c) Data lines d) Address lines	C
118	Which register is used to generate the different control signals? a) PC b) MAR c) MBR d) IR	D
119	Which register is used to hold the address when either reading or writing? a) PC b) MAR c) MBR d) IR	B
120	Control memory is a) RAM b) ROM c) Virtual memory d) Cache memory	B
121	Micro programmed control unit is _____ than hardwired but _____ a) Cheaper, more error prone b) Faster, more error prone c) Less error prone, slower d) Faster, harder to change	C

122	The goals of both hardwired and micro program control unit is a) Access memory b) Generate control signals c) Access the ALU b) Cost a lot of memory	B
123	A micro-programmed control unit a) is faster than a hard wired control unit b) facilitates easy implementation of new instructions c) is useful when very small programs are to be run d) usually refers to the control unit of microprocessor	B
124	Control program memory can be reduced by a) Horizontal format b) Vertical format micro program c) Hardwired control unit d) None of the above	B
125	Hardwired control is usually done in a) RISC architecture b) CISC architecture c) Both a and b d) None of above	A

Signature of Faculty **Signature of HOD**